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Device embedding assembly technology – Part 2-10: Design specification for cavity substrate

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY -

Part 2-10: Design specification for cavity substrate

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The text of this Technical Specification is based on the following documents:

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY -

Part 2-10: Design specification for cavity substrate

1 Scope

This document provides a general specification for the design of cavity substrates.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194-2, Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies